



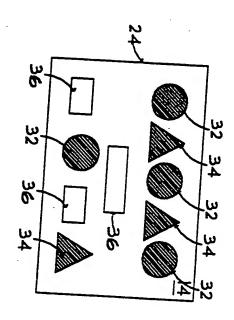
LAYER I SHAPED TO PERIMETER OF PCB

TOOLING PINS SWEDGED INTO LAYER 2

LAYER I

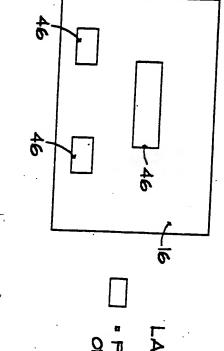
EITHER OR IS





" SMT CIT

SMT CUTOUT AREAS
AREAS
PTH COMPONENT CUTOUT
AREAS
PTH LEAD CUTOUT AREAS



FIGURE



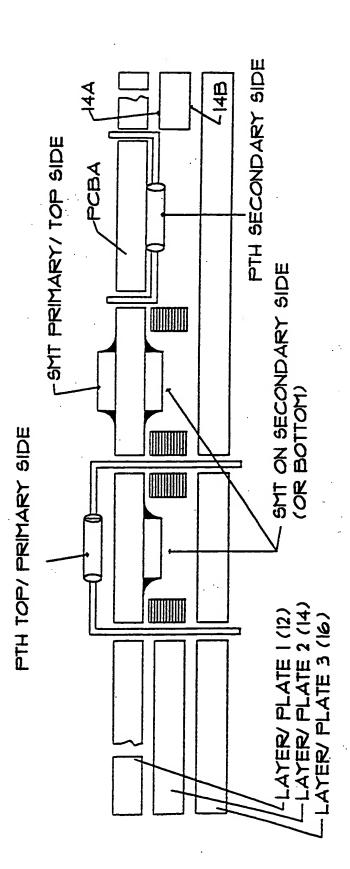


FIGURE 5



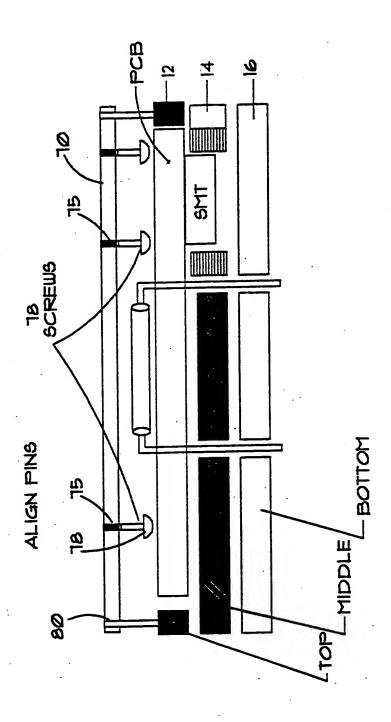
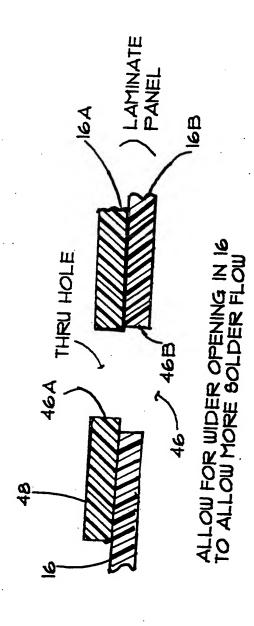


FIGURE 6





-IGURE 7

BOTTOP PLATE